08-2500

sPractitioner's Docket No. GR 97 P 1861 D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

DIVISIONAL APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventors:

VOLKER WEINRICH et al.

For (title):

Method of Producing an Electrode Configuration and Method of Electrically Contacting the Electrode Configuration

1. Type of Application

This new application is for a

[x] Divisional.
[ ] Continuation.
[ ] Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

[x] The new application being transmitted claims the benefit of prior U.S. application. Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for Filing Date under 37 C.F.R. 1.53(b)

19 Pages of Specification
5 Pages of Claims
4 Sheets of Drawing
[x] Formal
[ ] Informal

B. Other Papers Enclosed

__1__ Page of Abstract
____ Other

4. Additional Papers Enclosed

[ ] Preliminary Amendment
[x] Information Disclosure Statement (37 C.F.R. 1.98)
[x] Form PTO-1449 (PTO/SB/08A and 08B)
[ ] Citations
[ ] Declaration of Biological Deposit
[ ] Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
[ ] Authorization of Attorney(s) to Accept and Follow Instructions from Representative
[ ] Special Comments
[ ] Other

5. Declaration or Oath

[x] Enclosed
Executed by
[x] inventors.

6. Inventorship Statement

The inventorship for all the claims in this application are:

[x] The same.

7. Language

[x] English

8. Assignment

[x] An assignment of the invention to Infineon Technologies AG

[ ] is attached. A separate [ ] "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or [ ] FORM PTO 1595 is also attached.
[x] will follow.
[ ] was filed in parent application No.

9. **Certified Copy**

Certified copies of applications

GERMANY	197 28 474.4	July 3, 1997
Country	Application No.	Filed

from which priority is claimed

[ ] is (are) attached.
[ ] will follow.
[x] was filed in parent application No. 09/110,052

11. **Fee Payment Being Made at This Time**

[x] Enclosed

[x]	Filing fee	$690.00
	Total Fees Enclosed	$690.00

12. **Method of Payment of Fees**

[x] Check in the amount of $690.00.

15. **Authorization to Charge Additional Fees**

[x] The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 12-1099.

[x] 37 C.F.R. 1.16(a), (f) or (g) (filing fees)

[x] 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)

[x] 37 C.F.R. 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

[x] 37 CFR 1.17(a)(1)-(5) (extension fees pursuant to § 1.136(a).

[x] 37 C.F.R. 1.17 (application processing fees)

[ ] 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

16. Instructions as to Overpayment

[x] Credit Account No. 12-1099.

[ ] Refund

SIGNATURE OF PRACTITIONER

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Date of Deposit: August 24, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

ALEXIA VRAHIMIS

[x] **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

[x] Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added 1

[x] Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added 6

[ ] Plus added pages deleting names of inventor(s) named on prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added _____

[ ] Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

[ ] **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

[ ] This transmittal ends with this page.

ADDED PAGE FOR SPECIAL COMMENTS FOR NEW APPLICATION TRANSMITTAL

This divisional application claims the benefit under 35 U.S.C. § 120 of U.S. application No. 09/110,052, filed July 3, 1998

GR 97 P 1861 D

METHOD OF PRODUCING AN ELECTRODE CONFIGURATION AND METHOD OF ELECTRICALLY CONTACTING THE ELECTRODE CONFIGURATION

Background of the Invention:

Field of the Invention:

The present invention relates to a method of producing an electrode configuration and a method of electrically contacting the electrode configuration.

In the development of highly integrated memory modules, such as DRAMs and FRAMs, for example, the cell capacity should be retained or even improved in spite of the progressive miniaturization. In order to achieve this object, ever thinner dielectric layers and folded capacitor electrodes (trench cell, stack cell) are used. Recently, new materials, in particular paraelectric and ferroelectric materials, have been used between the capacitor electrodes of a memory cell, instead of the conventional silicon oxide. For example, barium strontium titanate (BST, $(Ba,Sr)TiO_3$), lead zirconate titanate (PZT, $Pb(Zr,Ti)O_3$) and/or lanthanum-doped lead zirconate titanate or strontium bismuth tantalate (SBT, $SrBi_2Ta_2O_9$) are used for the capacitors of the memory cells in DRAMs and/or FRAMs.

These materials are thereby usually deposited on existing electrodes (bottom electrodes). Processing takes place at high temperatures, with the result that the materials of which the capacitor electrodes are normally composed, for example doped polysilicon, are easily oxidized and lose their electrically conductive properties, which would lead to the failure of the memory cell.

Because of their good resistance to oxidation and/or because of the formation of electrically conductive oxides, 4d and 5d transition metals, in particular platinum metals (Ru, Rh, Pd, Os, Ir, Pt) and in particular platinum itself, and also rhenium are promising candidates which could replace doped polysilicon as electrode material in the above-mentioned memory cells.

In order to be able to construct a memory cell from the aforesaid materials, which have not been previously used in semiconductor technology, thin layers of these materials must be structured.

The structuring of the previously used materials is carried out as a rule by means of so-called plasma-supported anisotropic etching methods. Here, physical/chemical methods are usually applied in which gas mixtures composed of one or more reactive gases are used, such as oxygen, chlorine,

bromine, hydrogen chloride, hydrogen bromide and/or halogenated hydrocarbons and of inert gases (for example Ar, He). These gas mixtures are conventionally excited in an alternating electromagnetic field at low pressures.

Fig. 7 shows the principles of the method of operation of an etching chamber, illustrated for the example of a parallel-plate reactor 20. The gas mixture, for example Ar and Cl_2, is fed into a reactor chamber 22 through a gas inlet 21 and pumped out through a gas outlet 29. The lower plate 24 of the parallel plate reactor is connected to a high-frequency source 28 via a capacitor 27. The lower plate 24 serves as a substrate holder. By applying a high-frequency alternating electric field to the upper and lower plates 23, 24 of the parallel-plate reactor, the gas mixture is converted into a plasma 25. Since the mobility of the electrons is greater than that of the gas cations, the upper and the lower plates 23, 24 become negatively charged with respect to the plasma 25. For this reason, both plates 23, 24 exert a high force of attraction on the positively charged gas cations, with the result that they are subjected to a permanent bombardment by these ions, for example Ar^+. Since, in addition, the gas pressure is kept low, typically 0.1 - 10 Pa, there is only a low degree of scattering of the ions with respect to one another and to the neutral particles, and the ions strike virtually perpendicular against the surface of a substrate 26

which is secured to the lower plate 24 of the parallel-plate reactor. The result is that an image of a non-illustrated mask is formed on the underlying layer of the substrate 26 which is to be etched.

Photoresists are conventionally used as mask materials. Such resists can be structured relatively simply by means of an exposure step and a development step.

The physical part of the etching is brought about by means of the momentum and kinetic energy of the incident ions (for example Cl_2^+, Ar^+). In addition, chemical reactions between the substrate and the reactive gas particles (ions, molecules, atoms, radicals) are initiated or promoted (chemical part of the etching) thereby, accompanied by the formation of volatile reaction products. These chemical reactions between the substrate particles and the gas particles are responsible for high selectivities of the etching process.

Unfortunately, it has become apparent that the above-mentioned materials, which have newly been brought into use in memory cells, are among those materials which cannot be etched or can be etched dry-chemically only with difficulty. Further, the etching erosion is based, even when "reactive"

gases are used, predominantly or almost exclusively on the physical component of the etching.

Due to the fact that the chemical component of the etching is near negligible or absent, the etching erosion of the layer to be structured is of the same order of magnitude as the etching erosion of the mask and/or of the substrate (etching barrier layer), i.e. the etching selectivity with respect to the etching mask and/or substrate is generally small (between approximately 0.3 and 3.0). The result of this is that due to the erosion of masks with inclined edges and the unavoidable formation of facets on the masks only a low degree of dimensional accuracy of the structuring can be ensured.

The aforesaid problems also occur with the structuring of the top electrode of a memory cell which is constructed according to the "capacitor over bitline" principle with a so-called "stacked capacitor."

Furthermore, the use of a "stacked capacitor" leads to difficulties when making contact with the memory cell. In order to connect the memory cell to a metalization, contact holes of different depths have to be etched into an insulation layer arranged over and around the capacitor. This contact-hole etching should thereby stop at different depths in a way which is selective to different materials. In order

to simplify the manufacturing process, the use of only one mask level is to be aimed at.

In a memory cell according to the "capacitor over bitline" principle with a "stacked capacitor", the contact-hole etching must firstly stop at the material of the top electrode of the capacitor. Correspondingly, the material of the top electrode is the material which is subjected to the greatest degree of over-etching, while other contact holes are further etched to lower lying layers. If the top electrode is composed, for example, of platinum, there may occur, in addition to a break-through of the top electrode also a redeposition of sputtered platinum on the inner walls of the mask opening. This leads to so-called "fences", i.e. thin and conductive structures which remain even after the resist mask has been burnt off. These can lead to short circuits.

Summary of the Invention:

It is accordingly an object of the invention to provide a method of producing the electrode configuration, and a method of electrically contacting the electrode configuration, which overcomes the above-mentioned disadvantages of the prior art devices and methods of this general type.

With the foregoing and other objects in view there is provided, in accordance with the invention, an electrode configuration, comprising:

a first conductive layer of a material which is substantially unetchable by chemical dry-etching; and

a second conductive layer on the first conductive layer, the second conductive layer being formed of a material which is etchable, at least with a relatively low etching rate, by chemical dry-etching.

In other words, an electrode configuration is provided which has a first conductive layer, whose material is virtually impossible to etch by means of chemical dry-etching, and at least one second conductive layer whose material can be etched, at least with a low etching rate, by means of chemical dry-etching.

Here, chemical dry-etching is to be understood as a customary chemical dry-etching using, possibly excited, halogens, hydrogen halides or halogenated hydrocarbons or using oxygen at customary temperatures and gas pressures. In addition, a material which is virtually impossible to etch by means of chemical dry-etching is to be understood to be a material which, under process conditions which are optimum for the

respective material, has an etching rate of less than 1 nm/min. Correspondingly, a low etching rate is to be understood to be an etching rate which is greater than 1 nm/min under process conditions which are optimum for the respective material.

Since the material of the first layer is virtually impossible to etch by means of a chemical dry-etching, during a customary chemical/physical dry-etching the first layer is predominantly eroded by the physical part of the chemical/physical dry-etching. In contrast to this, during a customary chemical/physical dry-etching the second layer is also eroded by the chemical part of the chemical/physical dry-etching.

The invention has the advantage that the effective thickness of the electrode configuration can be increased by the height of the second layer, with the result that breaking through during the overetching when making contact with the electrode configuration is avoided. Likewise, the formation of redepositions from the material of the first layer during the overetching, which are difficult to remove, is prevented.

In addition, the layer resistance of the electrode configuration is reduced by the second layer of the electrode configuration - with an approximately constant capacity. As a

result, the switching of the so-called "common plate" during the so-called "pulsed-plateline" operation of the memory cell is speeded up, as a result of which the access time of the entire module is shortened.

Furthermore, the second layer of the electrode configuration permits the capacitor of the memory cell to be encapsulated with an oxide layer.

In accordance with an added feature of the invention, the first conductive layer contains a material selected from the group consisting of a 4d transition metal, a 5d transition metal, a conductive nitride thereof, and a conductive oxide thereof.

In accordance with another feature of the invention, the first conductive layer contains a material selected from the group consisting of ruthenium, rhodium, palladium, osmium, iridium, platinum, gold, silver and rhenium.

In accordance with an additional feature of the invention, the second conductive layer contains a material selected from the group consisting of aluminum, titanium, tungsten, a conductive silicide thereof, a conductive nitride thereof, and a conductive oxide thereof.

In accordance with a further feature of the invention, the second conductive layer contains a material selected from the group consisting of titanium and titanium nitride, preferably TiN_x where $0.8 < x < 1.2$.

With the above and other objects in view there is also provided, in accordance with the invention, a method of producing an electrode configuration, which comprises the following steps:

forming a first conductive layer of a material which is substantially unetchable by chemical dry-etching;

forming a second conductive layer on the first conductive layer from a material which is etchable, at least with a relatively low etching rate, by chemical dry-etching;

structuring the second conductive layer to form a structured second layer; and

dry etching the first conductive layer of the electrode configuration while using the second structured layer as a mask.

The invention has the advantage that the metals, metal silicides, metal nitrides or metal oxides of the second layer are more resistant in comparison with photoresists, with the

result that chemical "burning off" of the mask is prevented. The high bonding energy of the metal atoms in metals and/or the metal ions in silicides, nitrides or oxides leads to very low erosion rates during etching processes with a high physical component. The overall result of this is that the selectivity of the etching process of the first layer is increased. The lower mask erosion results in a higher dimensional accuracy of the structuring. Furthermore, the method according to the invention also permits steeper etching edges to be obtained on the layer to be structured by means of reactive gases.

In accordance with again an added feature of the invention, the dry etching step comprises etching the first layer with a plasma etching process.

In accordance with again another feature of the invention, during the dry etching step, at least one reactive substance is provided which reacts with the material of the second layer to form a non-volatile compound on the surface of the second layer. The reactive substance is preferably a reactive gas, such as oxygen (O_2), nitrogen (N_2), hydrogen (H_2), halogens, gaseous halogen compounds, or mixtures thereof. In this way, the chemical part of a chemical/physical dry-etching procedure is reduced and the etching erosion is

determined essentially by the physical portion of the etching.

In accordance with again an additional feature of the invention, an inert gas (e.g. argon) is provided during the step of dry etching the first layer.

The dry etching is effected with reactive ion etching (RIE), magnetically enhanced reactive ion etching (MERIE), electron cyclotron resonance etching (ECR), and inductively coupled plasma etching (ICP, TCP).

With the above objects in view there is also provided, in accordance with the invention, a method of electrically contacting an electrode configuration, which comprises the following steps:

forming an electrode configuration with a first conductive layer of a material which is substantially unetchable by chemical dry-etching, and a second conductive layer on the first conductive layer formed of a material which is etchable, at least with a relatively low etching rate, by chemical dry-etching;

applying at least one insulation layer on the electrode configuration, and structuring the insulation layer to form at least one contact hole to the electrode configuration; and

depositing a conductive layer and filling in the contact hole.

In accordance with yet an added feature of the invention, the insulation layer is a silicon oxide layer produced, for example, by a TEOS process or a silane process. The insulation layer may also contain a silicon layer.
In accordance with a concomitant feature of the invention, the conductive layer is formed of aluminum, tungsten, or copper.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a method of producing an electrode configuration and a method of electrically contacting the electrode configuration, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Figs. 1 to 3 are schematic side views illustrating a novel method for producing an electrode configuration according to the invention;

Figs. 4 to 6 are schematic side views illustrating a novel method of electrically contacting the electrode configuration; and

Fig. 7 is a schematic illustration of an etching chamber in the form of a parallel-plate reactor.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Figs. 1 to 3 thereof, there is seen a sequence of process steps leading to an electrode configuration according to the invention. Within the framework of the normal process control, oxide is repeatedly deposited on a silicon substrate 1, with the result that, finally, an oxide layer 2 which is up to 2 mm thick is

produced. A titanium layer 3 applied to the oxide layer 2 serves as barrier material for the subsequent platinum layer 4. The platinum layer 4 then serves as the bottom electrode for the capacitor of a memory cell and is therefore provided with a non-illustrated contact. The platinum layer 4 can be formed, for example, by sputtering. Then, the platinum layer 4 and the titanium layer 3 are structured. The structuring of the platinum layer 4 can be carried out by means of a TiN hard mask, analogously to the structuring of the top electrode described below. However, in the case of the platinum layer 4 (bottom electrode), the TiN hard mask is removed after the structuring. The resulting structure is shown in Fig. 1.

Subsequently, a barium strontium titanate layer 5 (BST, $(Ba,Sr)TiO_3$) is applied to the structure shown in Fig. 1. This layer is used later in the complete memory cell as a dielectric of the memory capacitor. A further platinum layer 6 is applied to the barium strontium titanate layer 5 as first conductive layer of the electrode configuration according to the invention. Then, a titanate nitride layer 7 is produced, as second conductive layer of the electrode configuration 10 according to the invention, on the platinum layer 6. The resulting structure is shown in Fig. 2.

The titanium nitride layer 7 is then structured by means of a phototechnique, in order to be able to serve as a "hard mask" for structuring the platinum layer 6 and the barium strontium titanate layer 5.

Then, reactive ion etching (RIE) is carried out in order to subject the platinum layer 6 to chemical/physical dry-etching. The etching gas used here is oxygen O_2 or a mixture of O_2 and further gases, for example argon. Instead of the reactive ion etching, other dry-etching methods, such as ion etching, magnetically enhanced reactive ion etching (MERIE), ECR (Electron Cyclotron Resonance) etching or inductively coupled plasma etching methods (ICP, TCP) can also be used, for example.

During the dry-etching of the platinum layer 6, non-volatile titanium oxide layers (Ti_xO_y) are continuously reformed on the surface of the titanium nitride mask 7, as a result of which the etching rate of the titanium nitride mask 7 is reduced still further. Correspondingly, the selectivity of the etching process is thus significantly increased. The associated lower degree of mask erosion thus results in a higher dimensional accuracy of the structuring. A suitable selection of the O_2 concentration makes it possible to set the edge angle of the etched edge on the platinum layer 6 over a wide range. In this way, the electrode configuration

according to the invention can be produced with a high degree of dimensional accuracy.

If the regions of the platinum layer 6 which are not protected by the titanium nitride mask are removed, the corresponding regions of the barium strontium titanate layer 5 are subjected to the reactive ion etching. Again, the etching gas used here is oxygen O_2 or a mixture of O_2 and further gases, for example argon. The titanium nitride hard mask 7 is thereby "hardened" further.

Instead of the reactive ion etching, other dry-etching methods, such as for example ion etching, magnetically enhanced reactive ion etching (MERIE), ECR (Electron Cyclotron Resonance) etching or inductively coupled plasma etching methods (ICP, TCP) can also be used during the dry-etching of the barium strontium titanate layer 5. The structure which results after the dry-etching of the barium strontium titanate layer 5 is shown in Fig. 3.

The electrode configuration 10 according to the invention has the advantage that the titanium nitride layer 7 (second layer of the electrode configuration) causes the layer resistance of the entire electrode configuration 10 to be reduced, while the capacity remains approximately the same. As a result, the switching of the so-called "common plate" in the so-called

"pulsed-plateline" mode of the memory cell is speeded up, causing the access time of the entire module to be shortened.

Figs. 4 to 6 show a schematic illustration of a method according to the invention for making contact with the electrode configuration according to the invention.

A thin SiO_2 layer 8 is applied for insulation over the entire area of the structure shown in Fig. 3, for example by means of a TEOS process. Since the deposition of an oxide layer on platinum is problematic, the titanium nitride layer 7 (second layer of the electrode configuration) makes it possible to encapsulate the capacitor of the memory cell with an oxide layer. Then, a resist layer 9 is applied to the thin SiO_2 layer 8. The resulting structure is shown in Fig. 4.

At the points at which contact holes are to be produced later, the resist layer 9 is exposed. Then, the resist mask is developed, i.e. the exposed regions of the resist layer 9 are removed. The resulting structure is shown in Fig. 5.

Then, a plasma etching process is carried out in order to produce the contact holes 12 and 13. As a result of the different depths of the contact holes 12 and 13, the electrode configuration 10 according to the invention is subjected to long overetching.

However, the electrode configuration 10 according to the invention has, by virtue of the titanium nitride layer 7 (second layer of the electrode configuration), a greater thickness, with the result that breaking through of the electrode configuration 10 during the etching of contact holes is avoided.

Likewise, the formation of redepositions from the material of the first layer (platinum layer 6) during the overetching, which redepositions can be removed only with difficulty, is prevented.

Then, the resist layer 9 is removed, resulting in the structure shown in Fig. 6.

We claim:

1. A method of producing an electrode configuration, which comprises the following steps:

forming a first conductive layer of a material which is substantially unetchable by chemical dry-etching;

forming a second conductive layer on the first conductive layer from a material which is etchable, at least with a relatively low etching rate, by chemical dry-etching;

structuring the second conductive layer to form a structured second layer; and

dry etching the first conductive layer of the electrode configuration while using the second structured layer as a mask.

2. The method according to claim 1, wherein the dry etching step comprises etching the first layer with a plasma etching process.

3. The method according to claim 1, which comprises, during the dry etching step, providing at least one reactive substance which reacts with the material of the second layer to form a non-volatile compound on the surface of the second layer.

4. The method according to claim 3, wherein the reactive substance is a reactive gas.

5. The method according to claim 4, wherein the reactive gas is a gas selected from the group consisting of oxygen, nitrogen, hydrogen, halogens, gaseous halogen compounds, and a mixture thereof.

6. The method according to claim 1, which comprises providing an inert gas during the step of dry etching the first layer.

7. The method according to claim 1, wherein the dry etching step is performed with an etching process selected from the group consisting of reactive ion etching, magnetically enhanced reactive ion etching, electron cyclotron resonance etching, and inductively coupled plasma etching.

8. A method of electrically contacting an electrode configuration, which comprises the following steps:

forming an electrode configuration with a first conductive layer of a material which is substantially unetchable by chemical dry-etching, and a second conductive layer on the first conductive layer formed of a material which is

etchable, at least with a relatively low etching rate, by chemical dry-etching;

applying at least one insulation layer on the electrode configuration, and structuring the insulation layer to form at least one contact hole to the electrode configuration; and

depositing a conductive layer and filling in the contact hole.

9. The method according to claim 8, wherein the insulation layer is a silicon oxide layer.

10. The method according to claim 8, wherein the applying step comprises producing a silicon oxide layer by a TEOS process.

11. The method according to claim 8, wherein the applying step comprises producing a silicon oxide layer by a silane process.

12. The method according to claim 8, wherein the insulation layer contains a silicon layer.

13. The method according to claim 8, wherein the depositing step comprises depositing a material selected from the group consisting of aluminum, tungsten, and copper.

Claim 14. A method of producing an electrode configuration, which comprises the following steps:

forming a first conductive layer of a material which is substantially unetchable by chemical dry-etching;

forming a second conductive layer on the first conductive layer from a material which is etchable, at least with a relatively low etching rate, by chemical dry-etching;

structuring the second conductive layer to form a structured second layer; and

subsequently forming an insulation layer on the second conductive layer.

dry etching the second conductive layer while using the first structured layer as a barrier for the chemical dry-etching.

15. The method according to claim 14, wherein the dry etching step comprises etching the first layer with a plasma etching process.

16. The method according to claim 14, which comprises, during the dry etching step, providing at least one reactive substance which reacts with the material of the second layer to form a non-volatile compound on the surface of the second layer.

17. The method according to claim 16, wherein the reactive substance is a reactive gas.

18. The method according to claim 17, wherein the reactive gas is a gas selected from the group consisting of oxygen, nitrogen, hydrogen, halogens, gaseous halogen compounds, and a mixture thereof.

19. The method according to claim 14, which comprises providing an inert gas during the step of dry etching the first layer.

20. The method according to claim 14, wherein the dry etching step is performed with an etching process selected from the group consisting of reactive ion etching, magnetically enhanced reactive ion etching, electron cyclotron resonance etching, and inductively coupled plasma etching.

Abstract of the Disclosure:

The electrode configuration includes at least one structured layer. A mask is produced on the layer to be structured and the layer is dry etched. The mask is at least slightly etchable by dry etching. The mask contains a metal silicide, a metal nitride or a metal oxide.

MN/bb- 97p1861d.DOC//8/24/00

FIG 1

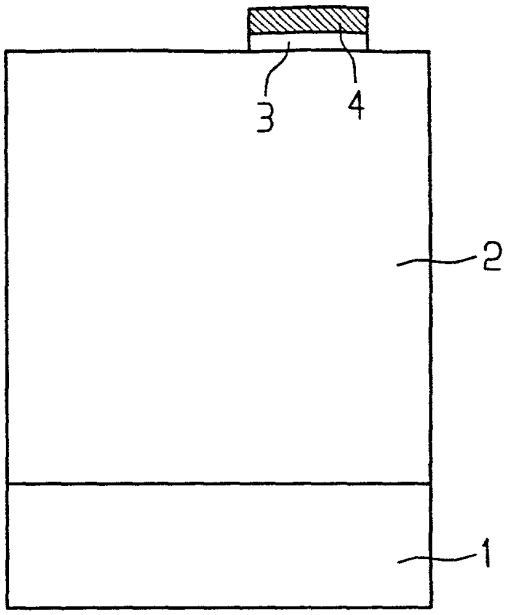


FIG 2

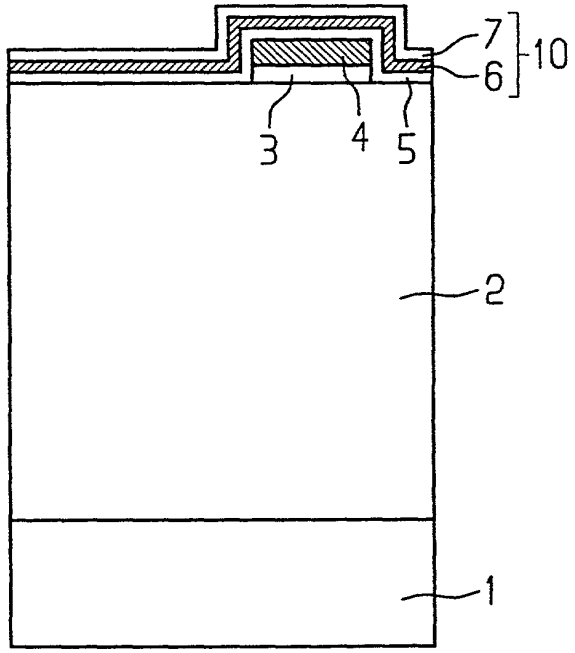


FIG 3

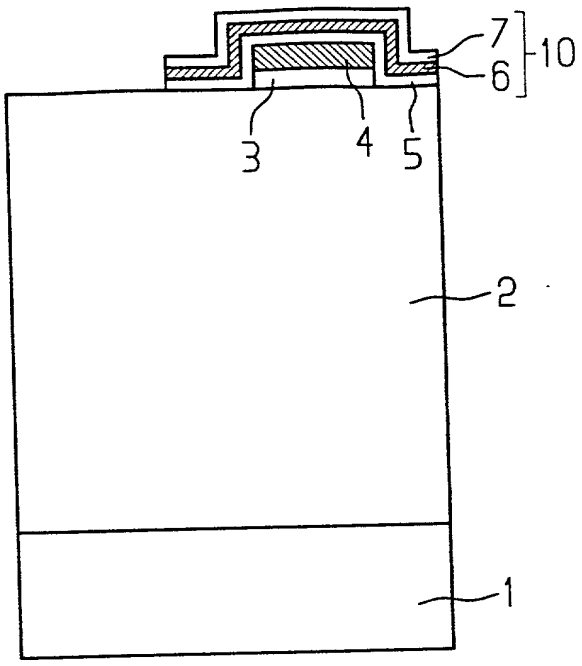


FIG 4

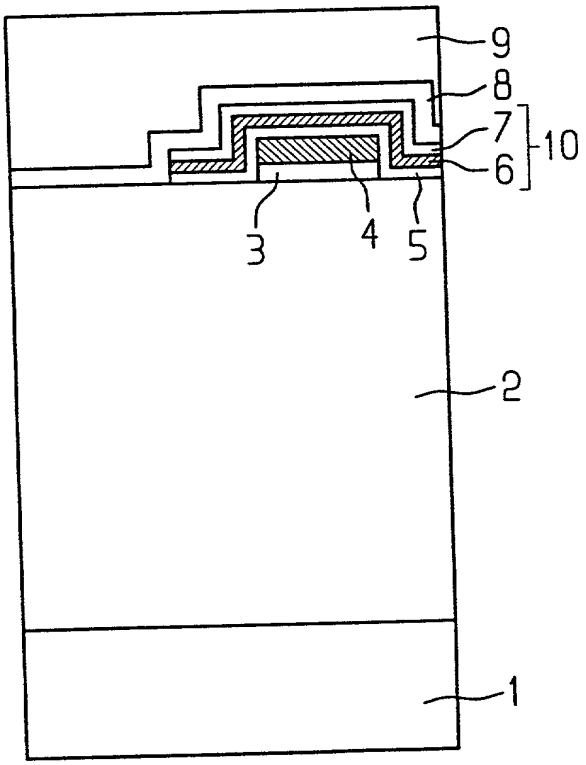


FIG 5

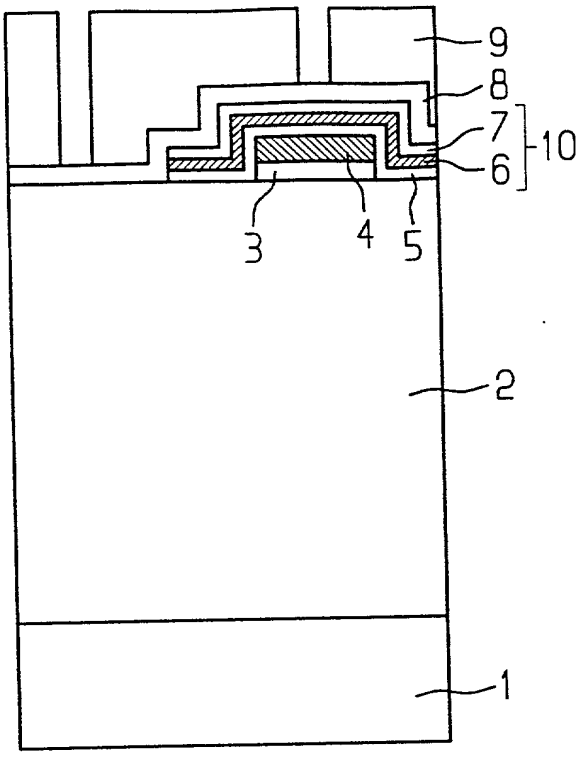


FIG 6

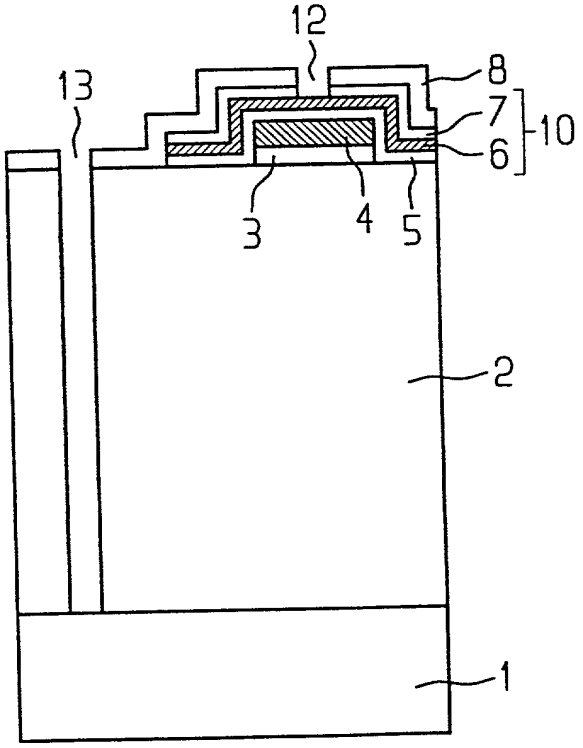
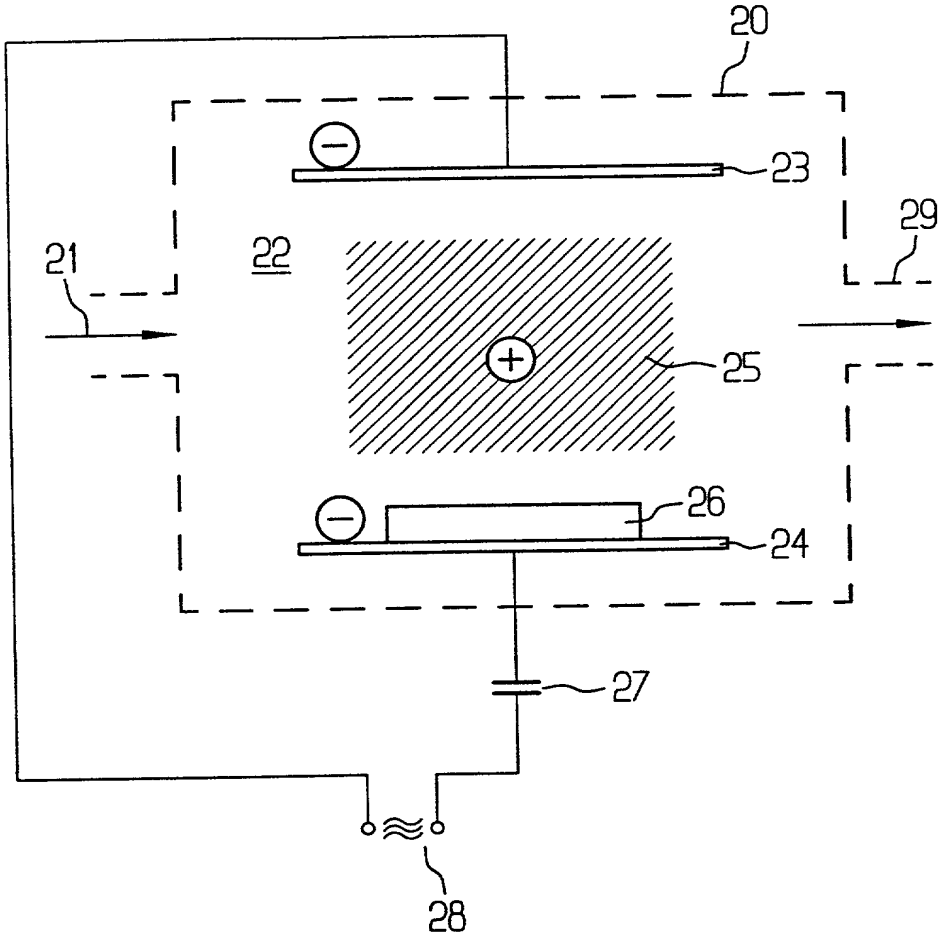


FIG 7



Docket No.: GR 97 P 1861

COMBINED DECLARATION AND POWER OF ATTORNEY IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRODE CONFIGURATION

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application Serial No. 197 28 474.4, filed July 3, 1997, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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